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Question Paper Code : X 60378

B.E./B.Tech. DEGREE EXAMINATIONS, NOV./DEC. 2020
Fourth Semester
Computer Science and Engineering
CS 2253/CS 43/CS 1252 A/080250011/10144 CS 404 – COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to Information Technology)
(Regulations 2008/2010)
(Also Common to PTCS 2253 – Computer Organisation and Architecture for B.E. (Part -Time) Third Semester – CSE – Regulations 2009)

Time : Three Hours Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. State the basic performance equation.
2. What do you mean by an interrupt ?
3. Compare hardwired and micro programmed controls.
4. What is nano programming ?
5. What is meant by hazard in pipelining ? Define data and control hazards.
6. Why is branch prediction algorithm needed ? Differentiate between the static and dynamic techniques.
7. Define access time.
8. Draw a block diagram to show the connections of the memory to the processor.
9. What is the use of DMA ?
10. What are the units of an interface ?

PART – B **(5×16=80 Marks)**

11. a) i) Explain different types of instructions with examples. Compare their relative merits and demerits. **(8)**

ii) Explain with an example how to multiply two unsigned binary numbers. **(8)**

(OR)

b) Explain the design of ALU in detail. **(16)**

12. a) Explain the following :

i) Address sequencing in control memory. **(8)**

ii) Micro program sequencer. **(8)**

(OR)

b) i) Explain multiple-bus organization. **(8)**

ii) Explain the design of hardwired control unit. **(8)**

13. a) Explain data hazard in detail. **(16)**

(OR)

b) Discuss the methods to reduce hazards due to conditional branches. **(16)**

14. a) i) Draw a block diagram to show the organization of a 8M × 32 memory using 512k × 8 memory chips. **(8)**

ii) A block - set - associated cache consists of a total of 64 blocks divided into 4-blocks sets. The main memory contains 4096 blocks, each consisting of 128 words. Find out how many bits are there in a main memory address. Also find out how many bits are there in each of the TAG, SET and WORD fields. **(8)**

(OR)

b) i) Explain the structure and modes of operation of synchronous DRAMs. **(10)**

ii) Write short notes on direct-mapped cache. **(6)**

15. a) What is an interrupt ? Explain the different types of interrupts and the different ways of handling interrupts. **(16)**

(OR)

b) i) Write and explain the working of Peripheral Component Interconnect (PCI) Bus. **(8)**

ii) Discuss DMA controller with block diagram. **(8)**